International Symposium on Digitally Assisted Analog & RF Circuit Design

Abstracts and short bios

“Introduction of Digitally Assisted Analog Circuit Design”

A. Matsuzawa (Tokyo Tech.)

Scaled CMOS provide excellent high frequency performance, however many analog performances; such as gain, linearity, mismatch, and noise looks become worse. Furthermore it is quite difficult to reduce occupied area in analog circuit and on-chip passive components, hence cost for analog portion will increase in mixed signal SoC. Conventional analog techniques can’t solve these issues effectively anymore and emerged digital assisted analog circuit design becomes attractive to address these issues. In my talk, I will review these current analog issues caused by CMOS technology scaling and will make overview of this emerged digital assisted analog circuit design technology.

Akira Matsuzawa received B.S., M.S., and Ph. D. degrees in electronics engineering from Tohoku University, Sendai, Japan, in 1976, 1978, and 1997 respectively. In 1978, he joined Matsushita Electric Industrial Co., Ltd. Since then, he has been working on research and development of analog and Mixed Signal LSI technologies; ultra-high speed ADCs, intelligent CMOS sensors, RF CMOS circuits, and digital read-channel technologies for DVD systems. He was also responsible for the development of low power LSI technology and SOI devices. From 1997 to 2003, he was a general manager in advanced LSI technology development center. On April 2003, he joined Tokyo Institute of Technology and he is professor on physical electronics. Currently he is researching in mixed signal technologies; RF CMOS circuit design for SDR and high speed data converters. He served a guest editor in chief for special issue on analog LSI technology of IEICE transactions on electronics in 1992, 1997, and 2003, and committee member for analog technology in ISSCC. Now he serves IEEE SSCS elected Adcom and IEEE SSCS Distinguished lecturer.

He received the IR100 award in 1983, the R&D100 award and the remarkable invention award in 1994, and the ISSCC evening panel award in 2003 and 2005. He is an IEEE Fellow since 2002.

“Software Defined Radio: The First Generation”

Asad A. Abidi (UCLA)

Recently completed research shows a plausible path to a highly integrated CMOS solution for software-defined radio. SDR is a versatile platform that can service, under software control, one from a wide range of bands (800 MHz – 3 GHz) and modulation schemes in both receive and transmit modes. We will describe a receiver based on a wideband front-end followed by a clock-programmable analog/digital back-end, that adapts to any reasonable channel bandwidth with strong on-chip attenuation of out-of-band blockers. We will also describe a transmitter based on a new realization of the outphasing architecture that can synthesize any widely used modulation in major bands with relatively high efficiency.

This SDR realization shows how intimately digital signal processing must combine with wideband analog circuits to achieve flexibility. This can be taken as a sign of things to come for all radios of the future.

Asad A. Abidi received the B.Sc.(Hon.) degree from Imperial College, London in 1976 and the M.S. and Ph.D. degrees in Electrical Engineering from the University of California, Berkeley in 1978 and 1981. He was at Bell Laboratories, Murray Hill, NJ from 1981 to 1984 as a Member of Technical Staff in the Advanced LSI Development Laboratory. Since 1985, he has been at the Electrical Engineering Department of the University of California, Los Angeles where he is Professor. He was a Visiting Faculty Researcher at Hewlett Packard Laboratories during 1989.

His research interests are in the design of CMOS RF integrated circuits, high-speed analog circuits, and data converters.

Dr. Abidi served as the Program Secretary for the International Solid-State Circuits Conference from 1984 to 1990 and as General Chairman of the Symposium on VLSI Circuits in 1992. He was Secretary of the IEEE Solid-State Circuits Council from 1990 to 1991, and from 1992 to 1995 he was Editor of the IEEE Journal of Solid-State Circuits. He has received the 1988 TRW Award for Innovative Teaching and the 1997 IEEE Donald G. Fink Award, the Jack Raper Award for Outstanding Technology.

“Digital RF Processor (DRP^{TM}) Technology to the Rescue: Why RF Can’t Exist without Digital Assistance Anymore?”

R. Bogdan Staszewski, (TI)

RF circuits, when implemented in nanoscale CMOS and, especially, when integrated in a larger SoC, suffer from numerous issues, such as poor linearity, device mismatch, low voltage headroom, high leakage, high flicker and substrate noise, etc. At the same time, the digital gates and memory are inexpensive yet powerful, so this mandates to use digital means to mitigate the RF circuit imperfections so that their adjusted performance can match or exceed that of traditional RF circuits. We examine opportunities of digital assistance of RF and then present case study of using Digital RF Processor (DRP) technology for digitally-friendly topological transformations, calibration due to process spread, compensation due to environmental changes, performance tuning, automatic reconfigurability, and built-in self-test.

R. Bogdan Staszewski received his PhD from the University of Texas at Dallas in 2002 for his research on RF frequency synthesis in digital deep-submicron CMOS. From 1991 to 1995, he worked at Alcatel Network Systems in Richardson, TX. He joined Texas Instruments in Dallas, TX, in 1995 where he holds an elected title of Distinguished Member of Technical Staff for his pioneering work on Digital RF Processor (DRPTM) architecture. He is currently a Chief Technical Officer (CTO) of the DRP system and design development group. He has authored and co-authored 80 journal and conference publications and holds 40 issued and 60 pending US patents.

"Digitally Assisted and Hybrid Architectures for RF Transceivers in Deep-Submicron CMOS"

JOEL L. DAWSON (MIT)

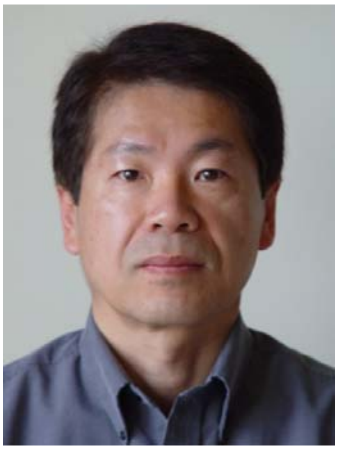
This presentation focuses on digitally assisted architectures for RF transceivers. Chief among the examples treated is a thorough analysis and characterization of a new power amplifier linearization architecture, with an exploration of its advantages and limitations. This architecture represents a new type of hybrid design for linearizers, in which functionality is optimally partitioned between the analog and digital domains. The idea centers on classic analog Cartesian feedback, using digital techniques to surmount the difficulties that have plagued Cartesian feedback in the past. Among these difficulties, perhaps the most severe is the need for high closed-loop bandwidth, which is impossible if a SAW filter is in the transmission path. Our hybrid architecture is innovative in that it does not require the closed-loop analog system to be fast. Our prototype maximally exploits this new degree of freedom.

JOEL L. DAWSON is an assistant professor in the Department of Electrical Engineering and Computer Science at MIT. He received the S.B. in EE from MIT in 1996, and the MEng. degree from MIT in EECS in 1997. He went on to pursue further graduate studies at Stanford University, where he received his Ph.D. in Electrical Engineering for his work on power amplifier linearization techniques. Before joining the faculty at MIT, Dr. Dawson spent one year at a startup company that he co-founded. He continues to be active in the industry as both a technical and legal consultant, having worked with BitWave Semiconductor, Nextwave Wireless, Fish and Richardson, and WilmerHale. Prof. Dawson received the NSF CAREER award in 2008.

"Digitally-Aided Analog Systems in the SOC Environment"

Bang-Sup Song (UCSD)

Aggressive device scaling down to the nano-meter range offers IC designers both opportunities and challenges. Digital designers may benefit greatly from the system flexibility and affordability, but analog/RF designers are struggling with flawed devices. Scaled devices are faster and smaller. An incentive to use such strengths advantageously has prompted many efforts to overcome analog imperfection by digital means. Designers are introducing more DSP functionality to enhance the analog and RF performance. Mixed-mode system chips will get smarter as more intelligence is built into analog/RF designs such as linear PA, RF receiver front-end, ADC/DAC, digital PLL, etc. Such pervasive design techniques with digital aiding will make a trend in the future SoC designs. Analog design suffers mostly from mismatch, non-linearity, and process variations. After a brief overview of the trend, examples of a few digitally-aided systems applied to image suppression, spurious-tone cancellation, filter time constant tuning, and ADC calibration will be presented.



Prof. Bang-Sup Song received the B.S. from Seoul National University in 1973, the M.S. from Korea Advanced Institute of Science in 1975, and the Ph.D. from University of California, Berkeley in 1983. From 1983 to 1986, he was a member of technical staff at AT&T Bell Laboratories, Murray Hill. From 1986 to 1999, he was a professor in the Department of Electrical and Computer Engineering and the Coordinated Science Laboratory, University of Illinois at Urbana. In 1999, he joined the faculty of the Department of Electrical and Computer Engineering, University of California, San Diego, where he is endowed with the Charles Lee Powell Chair Professor in Wireless Communication.

Prof. Song received a Distinguished Technical Staff Award from AT&T Bell Laboratories in 1986, a Career Development Professor Award from Analog Devices in 1987, and a Xerox Senior Faculty Research Award from the University of Illinois in 1995. His IEEE activities have been in the capacities of an Associate Editor and a Program Committee Member for IEEE Journal of Solid-State Circuits, Transactions on Circuits and Systems, International Solid-State Circuits Conference, and International Symposium on Circuits and Systems. He is an IEEE fellow.

“Digital Intensive/Calibrated Data Converter Design”

Tai-Cheng Lee (NTU)

CMOS technologies have progressed into nano-meter scale in the recent year, leading to the improvement of computing power of digital circuits. However, the scaling down of supply voltage and threshold voltage imposes the critical limitation of analog circuit design. Thus, the compatibility with CMOS deep-submicron technologies has emerged as important metrics in state-of-the-art ADC design.

In this talk, a couple techniques of pipelined data converter design are explored to optimize the performance. Additionally, with multiple data converters on the same chips, such as 802.11n and multiple-port Gigabit Ethernet, area-efficient with a background-calibrated DAC is proposed.

Tai-Cheng Lee was born in Taiwan, R.O.C., in 1970. He received the B.S.

degree from National

Taiwan University, Taipei, Taiwan, R.O.C., in 1992, the M.S. degree from Stanford University, Stanford, CA, in 1994, and the Ph.D. degree from the University of California, Los Angeles, in 2001, all in electrical engineering.

He was with LSI Logic from 1994 to 1997 as a Circuit Design Engineer.

Since 2002, he has been with the Department of Electrical Engineering and GIEE, National Taiwan University, where he is an Associate Professor. His main research interests are in high-speed mixed-signal and analog circuit design, data converters, PLL systems, and RF circuits.

“Design of Femtojoule Energy Efficient ADCs in CMOS”

Geert Van der Plas (IMEC)

In recent years significant energy efficiency improvements in A/D converters have been realized. A few years ago energy efficiencies of around 1pJ/conversion step were considered state-of-the-art, nowadays efficiencies down to fJ/conversion step are being reported.

In this talk the techniques and architectures will be explained that reduce the power consumption of data converters designed in nanometer CMOS processes for wireless applications. The talk will first introduce the basics of A/D converters, their performance specifications and typical architectures. Next the techniques used to improve energy efficiency will be introduced and examples of implementations will be given. These include fully dynamically clocked flash type converters with offset compensation that enables 50fJ/step data conversion for a 5b 1.75GS/s data converter. The passive charge sharing SAR A/D technique with noise reduction by redundancy similarly improves the energy efficiency to 54 fJ/step for a 9b 40MS/s design. And finally, a two-step architecture employing the CABS principle, which is a novel implementation of a successive approximation algorithm, improves the power efficiency to 10fJ/conversion step for a 7b 150MS/s converter.

All this will be explained in detail, with emphasis on design issues relevant for a successful implementation of the techniques.

Geert Van der Plas is Principal Scientist in the Wireless Research group of IMEC/NES. He obtained the M.Sc. and Ph.D. degrees from the Katholieke Universiteit Leuven, Belgium, in 1992 and 2001, respectively. From 1992 to 2001, he was a Research Assistant with the ESAT-MICAS Laboratory of the Katholieke Universiteit Leuven, where he worked in the field of mixed-signal design, modeling and design automation. In 2002, he was appointed as a Postdoctoral Research Assistant in the same research group. Since 2003, he has been with the Nomadic Embedded Systems division of the Interuniversitary Microelectronics Center (IMEC/NES), Belgium, where he has been working on signal integrity in mixed-signal systems and low-power scalable radios. He is currently coordinating the research on energy efficient data converters. He has been the author and co-author of over 75 papers in journals and conference proceedings.

“Digitally Assisted ADC Design”

Boris Murmann (Stanford Univ.)

Modern CMOS technologies provide digital signal processing capabilities at high integration density and low energy per operation. Hence, expending digital signal processing to enhance “irreplaceable” analog building blocks such as A/D converters has become a promising paradigm. In this presentation, we will review recent ideas in digitally assisted A/D conversion. Specific examples include pipeline ADCs with simplified residue amplifiers, digital distortion compensation in T/H circuits and pilot-tone based calibration schemes. The talk concludes by highlighting practical obstacles and the need for careful co-design and co-optimization of the underlying analog and digital blocks.

Boris Murmann is an Assistant Professor in the Department of Electrical Engineering, Stanford, CA. He received the Ph.D. degree in electrical engineering from the University of California at Berkeley in 2003. From 1994 to 1997, he was with Neutron Mikrolektronik GmbH, Hanau, Germany, where he developed low-power and smart-power ASICs in automotive CMOS technology. Dr. Murmann’s research interests are in the area of mixed-signal integrated circuit design, with special emphasis on data converters and sensor interfaces. He currently serves as a member of the International Solid-State-Circuits Conference (ISSCC) program committee. 'Design of femtojoule energy efficiency ADCs in CMOS'