

Mobility and strain characteristics in silicon nanowire FETs

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The silicon nanowire MOSFET is a promising structure for future VLSIs because of its high short channel effect immunity. When the width of nanowire is scaled down to the nanometer regime, transport properties are strongly affected by the quantum confinement effects. The transport is also affected by applying strain. In order to attain high performance nanoscale MOSFETs, the basic understandings of mobility, transport, strain effect, and band structures of silicon nanostructures are indispensable [1]. In this study, the width dependence of nanowire mobility [2,3] and strain effect [4] are investigated systematically and the physical origins of the measured electrical properties are discussed.

The devices were fabricated on (100) or (110) SOI wafer. After nanowire patterns are defined by the EB lithography and RIE, the nanowire width is further narrowed using SC1 solution. Then, BHF is used to over-etch the buried oxide (BOX) layer under the nanowires for gate-all-around (GAA) structure.

Fig. 1 shows measured electron mobility in nanowire nFETs on (110) SOI and width dependence of mobility [2]. The mobility is degraded in [100]/(110) nanowires as shrinking width, while narrower nanowires has higher mobility in [110]/(110) and is even higher than [110]/(110) bulk universal mobility. The observed mobility improvement in narrower [110]-nanowires on (110) can be explained by larger contribution from (100) sidewall that has higher electron mobility than (110) surface. This result indicates that the sidewall effect is one key point that affects mobility behavior as shrinking nanowire width.

The mobility behavior in pFETs is quite different. Fig. 2 shows measured hole mobility in nanowire pFET on (110) SOI [3]. In [100]-nanowire, comparable mobility with universal mobility is obtained even in a narrow nanowire. Moreover, very high mobility is observed in the high N_{inv} regime in [110]-nanowire although the device has (100) sidewall where hole mobility is low. The high mobility in the the high N_{inv} regime may be caused by higher carrier population on (110) surface than (100) due to strong carrier confinement.

Fig. 3 shows transverse tensile strain (~ 100 MPa) effects on drain current of nanowire FETs [4]. The current increases by strain in both nFETs and pFETs. Much larger current increase is observed in pFETs. The strain effects do not depends on nanowire width in nFET. However, it is found that strain effect in nanowire pFET depends on nanowire width because m^* modulation becomes smaller as decreasing nanowire width. More current improvement can be expected if relatively larger strain (\sim GPa) is applied.

In summary, mobility and strain effects in nanowire FETs are investigated. The understandings of nanowire transport and physics are essential for the design of nanowire FETs.

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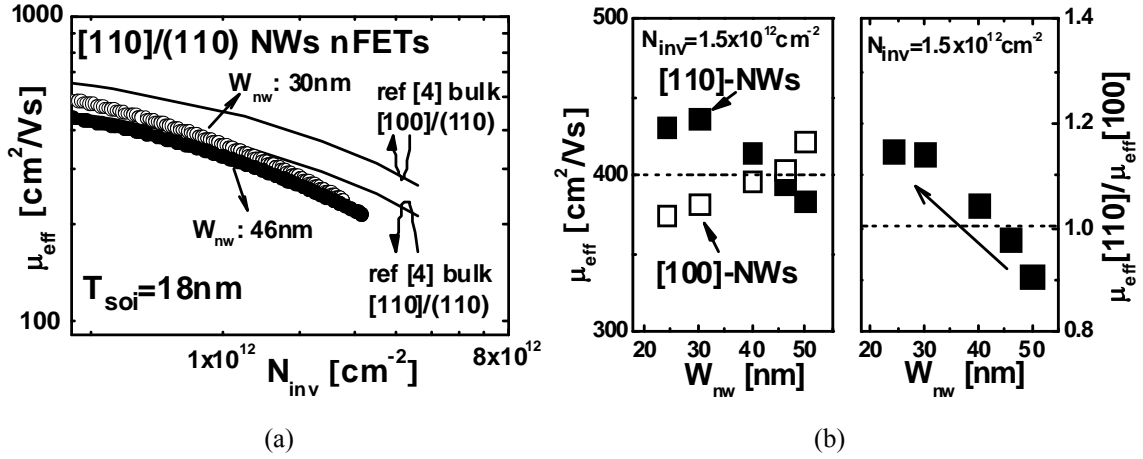


Fig. 1. Mobility in nanowire nFETs on (110). (a) Mobility in [110]/(110) nFETs. (b) Width dependence of mobility and mobility ratio of [110] to [100].

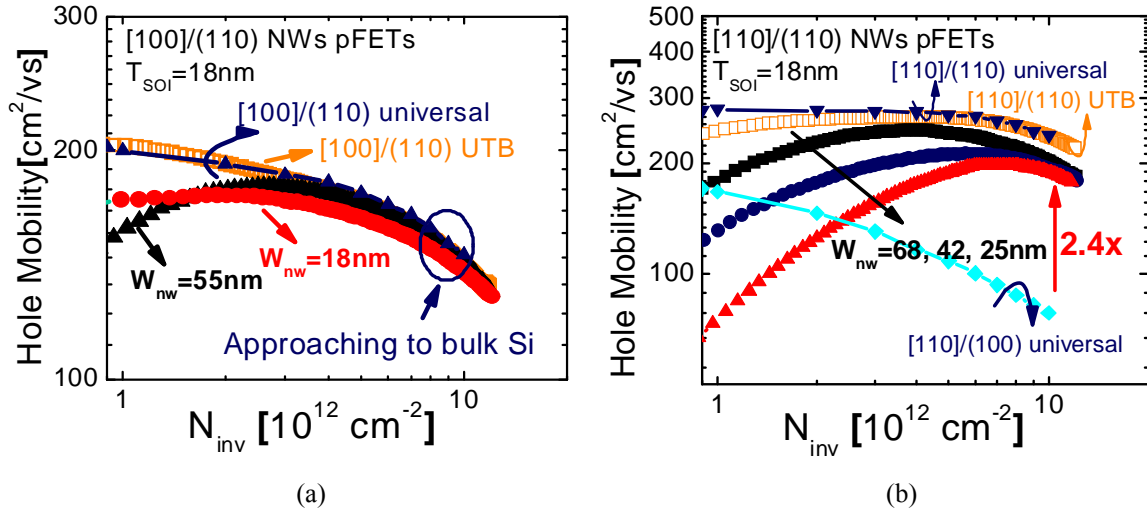


Fig. 2. Mobility in nanowire pFETs on (110). (a) Mobility in [100]/(110) pFETs. (b) Mobility in [110]/(110) pFETs.

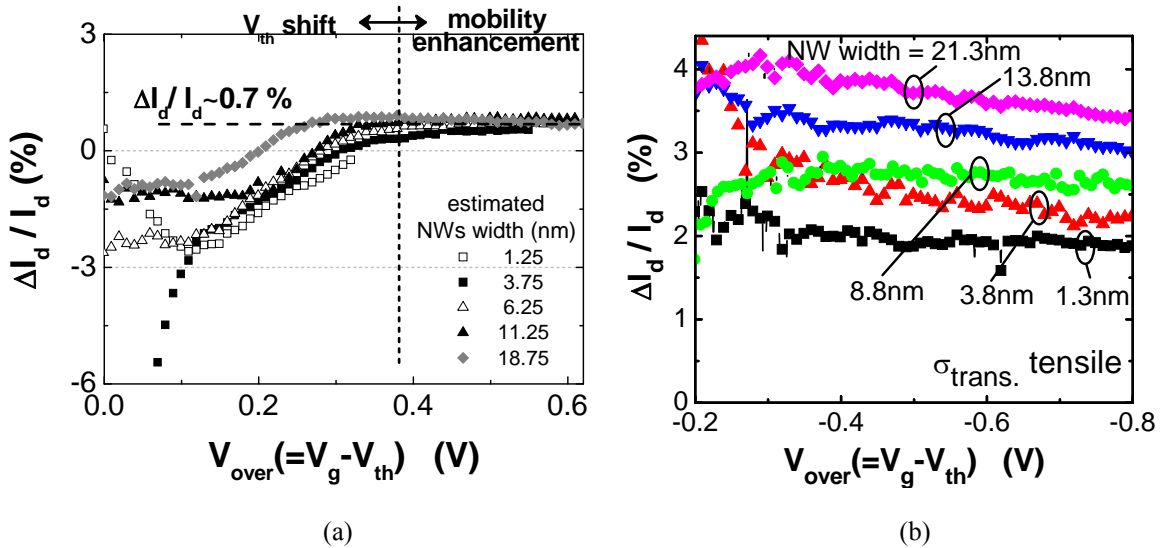


Fig. 3. $\Delta I_d/I_d - V_{over}$ characteristics of nanowire (a) nFETs and (b) pFETs on (100) under transverse tensile strain.