Fabrication and Characterization of Si and Heterojunction Tunnel Field Effect Transistors

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The stringent requirements imposed by the ITRS not only necessitate the implementation of advanced processing modules but also rely on the introduction of alternative and/or new gate concepts. Multi-gate devices such as FinFETs have paved the way to the introduction of Si nanowires. To further enhance the electrical performance one can go a step further and switch over to another operating principle of the devices. Quantum flux and spintronics are examples of possible future devices no longer based on the transport of electrical charges. However, a more direct extension of the present CMOS research is making use of tunnelFETs (TFETs), whereby band-to-band tunneling is used instead of thermo-ionic emission. These devices have a low subthreshold swing (< 60 mV/dec), reduced short-channel effects and enable the fabrication of 3D structures based on vertical nanowires. However, as the large Si bandgap leads to a low tunneling efficiency the achievable on-current is limited. Therefore, research has been triggered toward hetero-structures consisting of a Si drain and intrinsic region and a low bandgap material source such as e.g. Ge or even GaAs for n- and pTFET, respectively.

This presentation will focus on the TFET work on going at IMEC [1-3]. First some technological challenges for both vertical and horizontal devices are addressed. In a second part important aspects related to the device characterization are discussed. Recent results on multi-gate TFETs pointed out for these devices a point subthreshold swing of 46 mV/dec and an Ion/Ioff ratio of 10^6 for 25 nm wide devices at a supply voltage of 1.2 V. The tunnel efficiency depends on the fin width. Beside static device characteristics one also has to investigate the reliability aspects and the noise performance. Finally, some benchmarking will be done with state-of-the-art results reported in the literature.

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2) D. Leonelli, A. Vandooren, R. Rooyackers, A.S. Verhulst, S. De Gendt, M.M. Heyns and G. Groeseneken, presented at SSDM, Miyagi, Japan (2009)
3) A.S. Verhulst, W.G. Vandenberghe, D. Leonelli, R. Rooyackers, A. Vandooren, S. De Gendt, M.M. Heyns and G. Groeseneken, Proc. ULSI Process Integration 6, Trans. Electrochem. Soc., vol. 25(7) (2009).

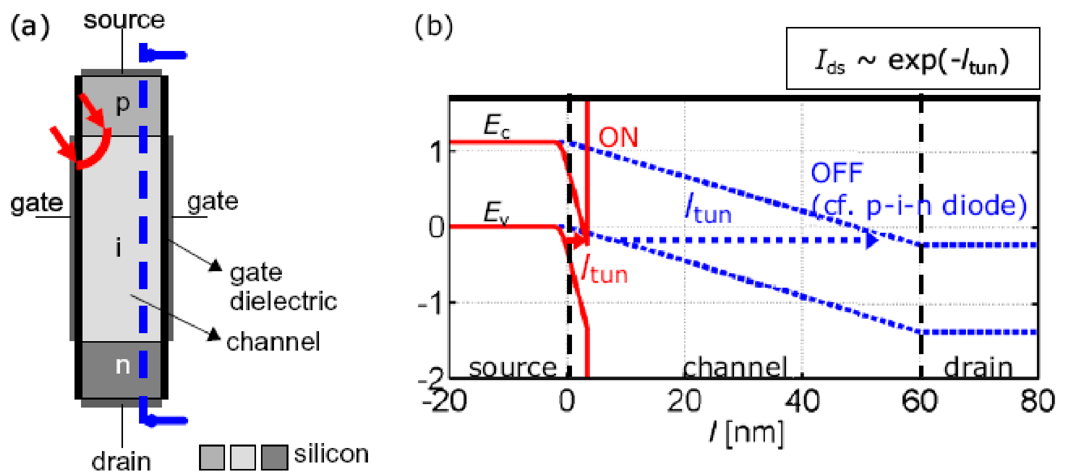

Fig. 1: (a) Schematic representation of the cross-section of a nanowire-based TFET. (b) Positions of the band edges along the cut-lines marked in (a), indicating the difference in tunnel-path length l_{tun} between the on-state and off-state of the TFET.

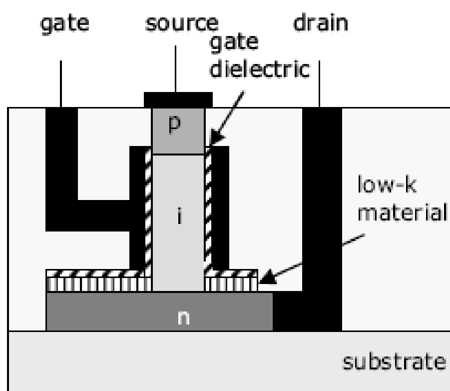

Fig. 2: Cross-section of a vertical nanowire based TFET w/o a gate to drain overlap to suppress the ambipolar behavior.

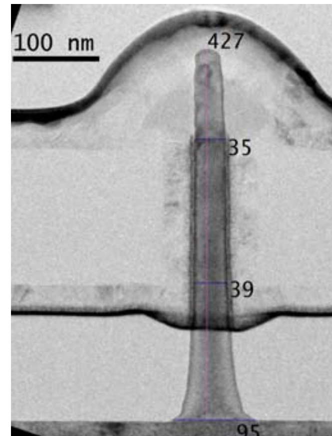

Fig. 3: TEM cross section of a 35 nm wide tunnel FET

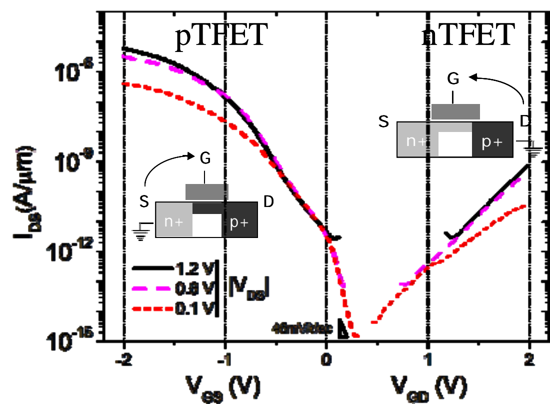

Fig. 4: p- and nTFET input characteristics for a MuGFET structure with a 25 nm wide fin (Lg=160 nm).

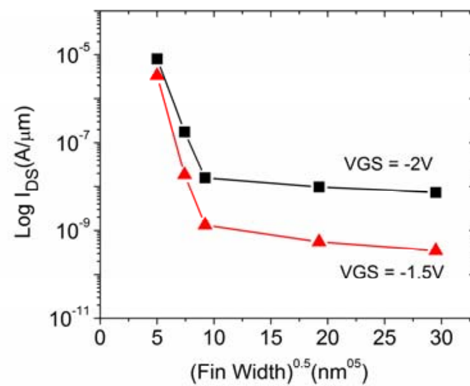

Fig. 5: Width dependence for different gate voltages, for a TFET with Lg=160 nm)