

New channel material MOSFETs on Si platform

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It has been well recognized that, under deep sub-100 nm regime, conventional device scaling concept has confronted with several physical and essential limitations. Therefore, any new device engineering to realize advanced CMOS is strongly needed for overcoming these difficulties. Particularly, the carrier-transport-enhanced channel MOSFETs have been regarded as strongly important for obtaining high current drive and low supply voltage [1]. From this viewpoint, attentions have recently been paid to III-V channels as a candidate of high performance n-MOSFETs beyond strained-Si devices. It is also known that Ge channels are suitable for p-MOSFETs, because of the highest hole mobility among principal semiconductors. On the other hand, MOSFETs using these materials must be fabricated on Si substrates in order to fully utilize Si CMOS platform. Thus, a possible ultimate CMOS structure is shown in Fig. 1 [1].

There are many technological issues to realize the Ge/III-V MOSFETs on Si substrates, which are listed as follows; (1) gate insulator formation with superior MOS/MIS interface quality (2) high quality Ge/III-V film formation on Si substrates (3) low resistivity source/drain formation (4) total CMOS integration. However, a significant progress has recently been made for gate stack technologies for Ge/III-V MOS interfaces. One typical structure exhibiting superior interface properties is a thermally-oxidized GeO_2/Ge interface. We have reported that this interface provides the interface state density less than $10^{11} \text{ cm}^{-2}\text{eV}^{-2}$ without any interface passivation annealing (Fig. 2) [2]. We have also demonstrated the inversion-layer hole mobility of as high as $575 \text{ cm}^2/\text{Vs}$ at maximum for p-MOSFETs using GeO_2/Ge as an interface layer (Fig. 3) [3].

One of the other difficult challenges is to form thin and high quality Ge/III-V films on Si. As for Ge-On-Insulator (GOI) structures, the Ge condensation technique [4] is a promising technology for fabricating thin GOI films on Si. We have demonstrated the successful fabrication of (110)-oriented GOI structures (Fig. 4) [5] and the device operation of (110) GOI pMOSFETs [6]. Higher mobility performance of (110) GOI p-MOSFETs than (100) ones has been obtained.

As for III-V materials, on the other hand, there can be two possible ways to form III-V thin films on Si or SiO_2/Si . One way is the micro selective growth of III-V materials on Si. We have fabricated III-V lateral overgrowth regions for planer III-V-OI MOSFETs and vertical nano-wire III-V MOSFETs, applicable to 3D integration by using InGaAs grown by MOVPE on (111) Si substrates [7], as shown in Fig. 5. The other way is the wafer bonding of Si and III-V substrates. We have also recently succeeded in fabricating $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ -on-Insulator substrates with smooth and flat interfaces (Fig. 6) and high electron mobility nMOSFET operation on this substrate (Fig. 7).

In summary, CMOS family utilizing SiGe/Ge channels and III-V channels can be key devices for high performance and low power advanced LSIs in the future. This work was partly supported by a Grant-in-Aid for Scientific Research on Priority Area (No. 18063005) from MEXT, NEDO/MIRAI project and Innovation Research Project on Nano electronics Materials and Structures from NEDO/METI. The authors would like to thank Prof. S. Sugahara in Tokyo Institute of Technology for his cooperation and support. The authors would also like to thank S. Dissanayake, Y. Nakakita, T. Sasada, H. Matsubara, T. Hoshii, M. Deura, Y. Kondo, T. Haimoto, K. Morii, S. Nakagawa, K. Tomiyama, T. Iwasaki, S. Kim, M. Shichijo, Dr. M. Yokoyama and Dr. R. Nakane in the University of Tokyo, Drs. T. Yasuda, N. Miyata, H. Ishii, T. Itatani in AIST, Drs. A. Ohtake in NIMS and Drs. M. Hata, N. Fukuhara and H. Yamada in Sumitomo Chemical for their collaborations.

References [1] S. Takagi et al., *Solid-State Electron.* 51, 526 (2007); S. Takagi et al., *IEEE TED* 55, 21 (2008) [2] H. Matsubara et al., *Appl. Phys. Lett.* 93, 032104 (2008) [3] Y. Nakakita et al., *IEDM*, 877 (2008) [4] S. Nakaharai et al., *Appl. Phys. Lett.* 83, 3516 (2003) [5] S. Dissanayake et al., *Thin Solid Films*, Vol. 517, 178 (2008) [6] S. Dissanayake et al., *Abs. ICSi-5*, 57 (2007); *Ext. Abs. SSDM* (2009) [7] T. Hoshii et al., *Phys. Stat. Sol. (c)* 5, 2733 (2008); M. Deura et al., *J. Crystal Growth* 310, 4768 (2008); M. Deura et al., *Appl. Phys. Exp.* 2, 011101 (2009) [8] M. Yokoyama et al., *VLSI symp.* (2009) 242

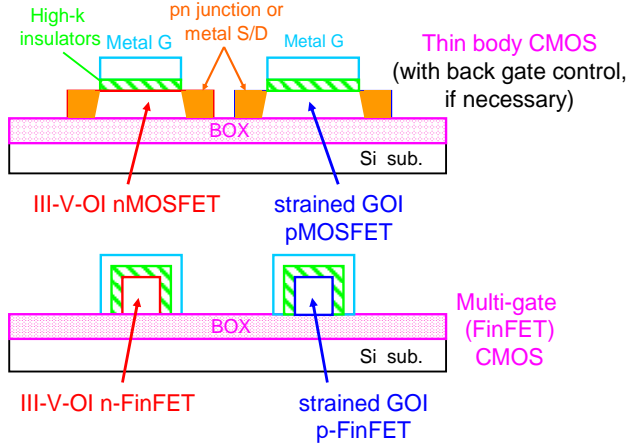


Fig. 1 Ultimate CMOS structure composed of the combination of III-V semiconductors n-MOSFETs and Ge p-MOSFETs on insulators

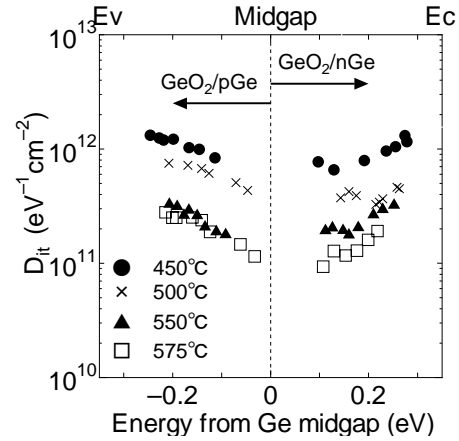


Fig. 2 Oxidation temperature dependency of the energy distribution of the interface state density for GeO₂/Ge interfaces

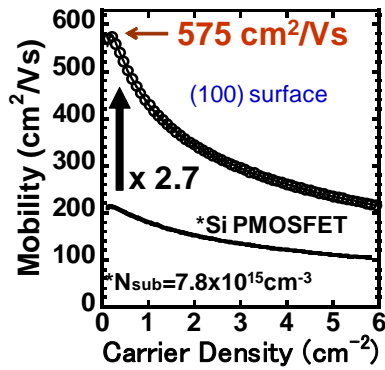


Fig. 3 Hole mobility of GeO₂/Ge p-MOSFETs as a function of N_s

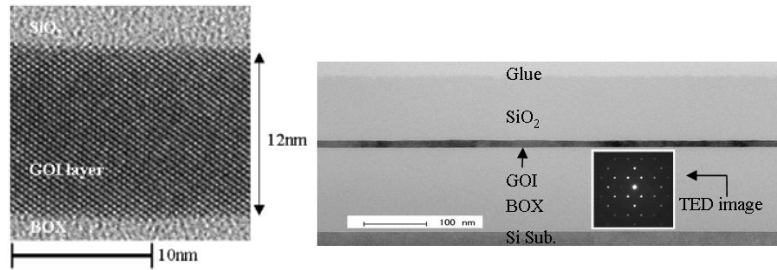


Fig. 4 Cross sectional TEM photographs of (110)-oriented Ge-On-Insulator structure fabricated by applying Ge condensation technique to (110) SOI substrates

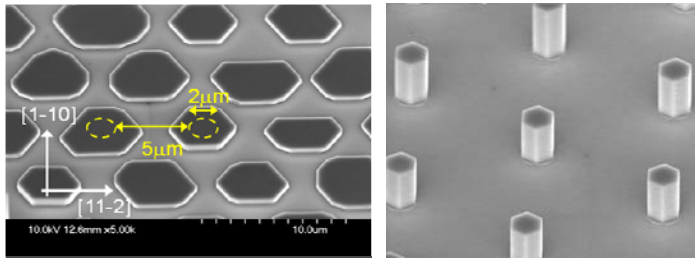


Fig. 5 Perspective SEM views of lateral (left) and vertical (right) InGaAs on (111) Si fabricated under different MOVPE growth conditions

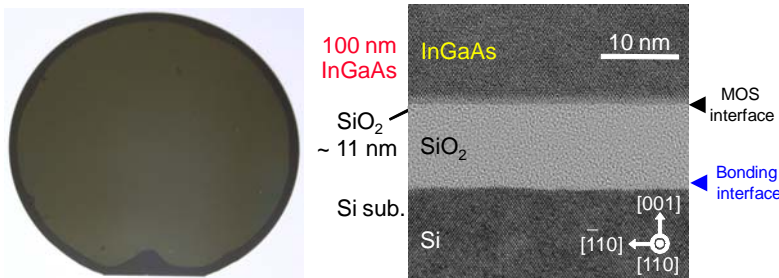


Fig. 6 2-inch InGaAs-on-insulator substrate fabricated by wafer bonding technique and TEM photograph of cross section of this substrate

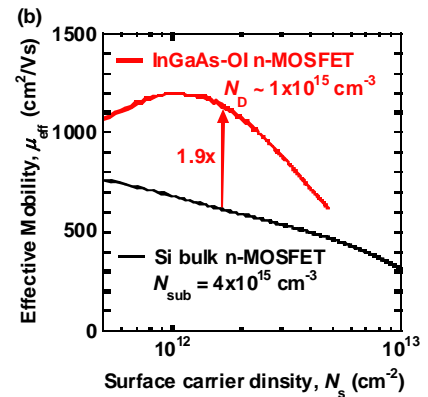


Fig. 7 Electron mobility of InGaAs-OI n-MOSFETs as a function of N_s