InGaAs/InP MISFET

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Introduction According to the ITRS 2007 report [1], the III-V semiconductor device technology can be potentially combined with the LSI technology to realize circuits that are better than the current CMOS circuits. The ITRS report states the future MOSFETs will have a high saturation drain current (I_d) of around 3 A/mm. To achieve such high I_d in MISFET with III-V channels, the source doping concentration must be higher than 1×10^{19} cm^{-3}, which has been estimated using a simple ballistic model [2]. Moreover, higher doping concentration is required to eliminate influence of parasitic resistance of source and drain (S/D) [3]. However, in the case of III-V materials, it is difficult to obtain a high source doping concentration using ion implantation techniques. On the other hand, maximum doping concentration by epitaxial growth is around 1×10^{20} cm^{-3}[4,5]. One of the solutions to this problem is to use MISFETs with regrown S/D [6] so that the transconductance (g_m) and I_d are high; such MISFETs can be used to realize high-speed and low-power-consumption devices. The other solution is vertical FET. In this report, we would like to report our approaches to realize epitaxially grown source. One approach is an InP/InGaAs composite channel MISFET with InGaAs S/D by selective regrowth of metalorganic vapor phase epitaxy (MOVPE) [7,8]. The other approach is vertical FET [9-11]. In case of vertical FET, hetero-launcher for ballistic transportation of electron was introduced [12,13].

Lateral MISFET with regrown S/D To fabricate regrown source, a slight overlap between the gate electrode and source is necessary for low access resistance. Thus channel region must be etched with undercut before the regrowth. To penetrate regrown source into undercut portion, we used MOVPE.Figure 1 shows a schematic of the cross section of regrown S/D MISFET. In this MISFET, all of structures were fabricate by photolithography. The length and width of the channel is 6 μm and around 20 μm, respectively. The device fabrication processes are as follows. At first, a 12-nm-thick InGaAs channel layer and a 5-nm-thick InP layer were grown on buffer structure by undoped InAlAs layer and undoped InP layer. Then 100-nm-thick SiO_2 dummy gate structures were fabricated on a thin InP layer. Afetr etching of S/D region with an undercut, the samples were immediately loaded into an MOVPE chamber and selective regrowth was carried out. After isolation of each device, the dummy gate was removed and was replaced with a 20-nm-thick gate insulator by PECVD. After formation of Al/Au gate electrodes, Ti/Pd/Au S/D electrodes were deposited. From cross-sectional SEM observation (Fig. 2), the undercut length was found to be approximately 48 nm, and it was found to be filled with regrown InGaAs without any voids. The thickness of the regrown layer was around 100 nm. The I_d–V_d and I_d–V_g characteristics of the fabricated regrown S/D MISFET are shown in Figs. 3 and 4. Figure 3 indicates clear gate voltage modulation and small current saturation. The maximum I_d is around 340 mA/mm (at $V_d = V_g = 3$ V), and g_m is around 43.6 mS/mm (at $V_g = 0.5$ V). An estimated mobility is 3,030cm^2/Vs.

Vertical MISFET with hetero-launcher In vertical FET, we used a combination of InGaAs/InP hetero-launcher and undoped InGaAs channel to achieve pure ballistic transportation. Electrons extracted from the hetero-launcher propagate without scattering only in the undoped channel. By estimating via the Monte Carlo simulation [12,13], cut-off frequency is over 1 THz when drain current density is over 1 MA/cm^2. At this point calculated electron velocity is over 7.5×10^7 cm/s. Schematic structure of fabricated devices is shown in Fig. 5. Fabrication processes are as follows. After growth of n-InP source and 120-nm-thick i-InGaAs channel by MOVPE, a 150-nm-thick and 60 nm-wide tungsten drain electrode was formed. After etching of the i-InGaAs layer and the n-InP layer by CH_4-H_2 ICP-RIE, wet etching by sulfuric acid solution and hydrochloric acid solution eliminated any damage by RIE. After deposition of the 10-nm-thick SiO_2 gate insulator by PECVD, a titanium gate was deposited by sputtering. To obtain isolation between drain electrode and gate metal, gate metal and gate insulator around the drain electrode were eliminated by a combination of photo-resist coating, etchback, and etching by BHF [14]. Then the mesa was completely immersed in a BCB insulating layer, followed by an etchback process to expose the drain electrode. Finally, a Cr/Au electrode pad was formed. The SEM image of fabricated gate stack is shown in Fig. 6. The I_d–V_d characteristics of the fabricated device that was designed 60 nm of source width and 5 μm of device length are shown in Fig. 7. As shown in Fig. 7, clear modulation and saturation of drain current were observed. The maximum drain current density was 1 A/mm. The I_d–V_g characteristic is shown in Fig. 8. As shown in Fig. 8, the value of the peak of g_m was 550 mS/mm.

Conclusion Toward heavily doped source straucture in InP/InGaAs MISFET, MISFET with regrown S/D and vertical FET were reported. It was confirmed that regrown InGaAs source was connected with channel by penetration of undercut region. I-V Characteristics shows feasibility of regrown source. Vertical MISFET with dual gate and hetero-launcher were also fabricated.

References

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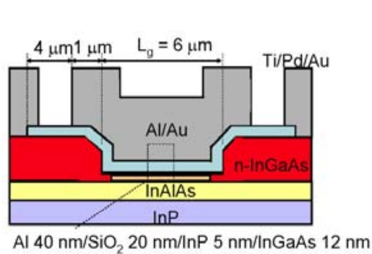

Fig.1 Schematic device structure of lateral MISFET with regrown S/D/

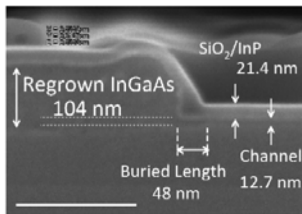

Fig.2 Cross-sectional SEM images of buried regrowth region after dummy gate removal and gate insulator deposition.

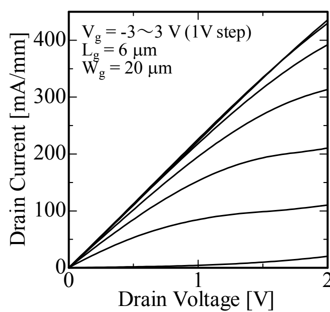

Fig.3 I_d–V_d characteristics of MISFET

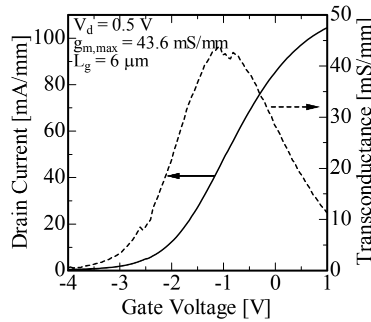

Fig.4 I_d–V_g characteristics of MISFET

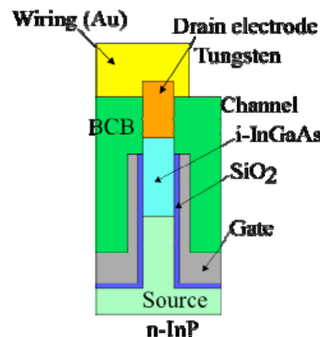

Fig. 5 Schematic image of device

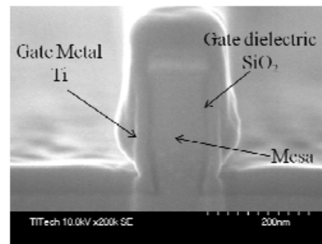

Fig. 6 The structure of gate stack

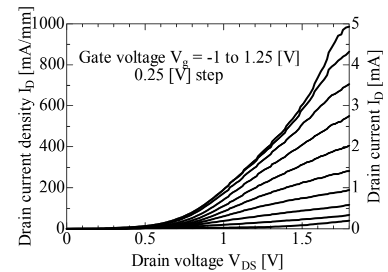

Fig. 7 I_d–V_d characteristics of vertical FET

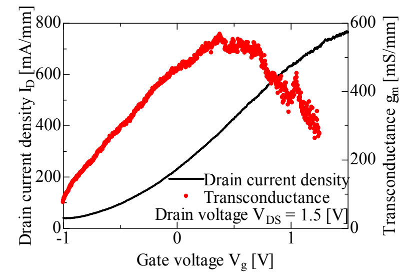

Fig. 8 I_d–V_g characteristic of vertical FET