Structures for Quantum Computing Using Coupled Silicon Quantum Dots

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Although most solid state proposals for quantum computation rely on the original ideas of Kane[1], many variations were suggested for many years and the realisation of a viable quantum bit still remains at an early stage[2]. The approach we have developed uses charge states in an isolated double quantum dot (IDQD) in silicon as the basis element for quantum information as well as a nearby single electron transistor (SET) that is used for charge readout[3]. Here we report on the detection of charge motion in the double dot system by single electron tunnelling or cotunnelling event in the SET. We have probed the charge state degeneracy of the IDQD and showed that the electron displacement in the IDQD is associated with a substantial charge rearrangement in the SET island and the existence of two stable ground states of the SET. Also back-action from the SET is observed and gives an estimate of the maximum measurement duration.

The devices were fabricated from a silicon-on-insulator (SOI) substrate with a 20 - 45 nm-thick silicon layer, doped with phosphorous at a density of $2.9\ 10^{19}$ cm^{-3}. High resolution electron beam lithography and reactive ion etching were used to pattern a single dot for the SET and the isolated double dot. The SET and the IDQD are controlled by in-plane gates within the same SOI layer. A custom low temperature complementary metal-oxide-semiconductor circuit is used to provide the various voltages to the device and to measure the SET current through a charge integrator circuit[4]. Several fabrication strategies are being employed, with the same general geometry, to assess the robustness of the approach.

SET current dependencies on SET and IDQD gates are complex but specific features associated with electron motion in the IDQD could be distinguished. These are characterised by an abrupt shift in gate voltage of a single Coulomb blockade peak. The shift is about 1/3 of the Coulomb blockade period, a value much larger than the currently predicted ones by capacitance calculations[5] but explained by a modification of the occupancy of localised states around the SET island. Indeed these trap states can control the coupling between the SET and the IDQD. Electron motion in the IDQD brings the SET into a degenerate state and SET back-action on the IDQD is negligible for timescale shorter than 10 ms suggesting that charge qubit computation is possible in these structures.

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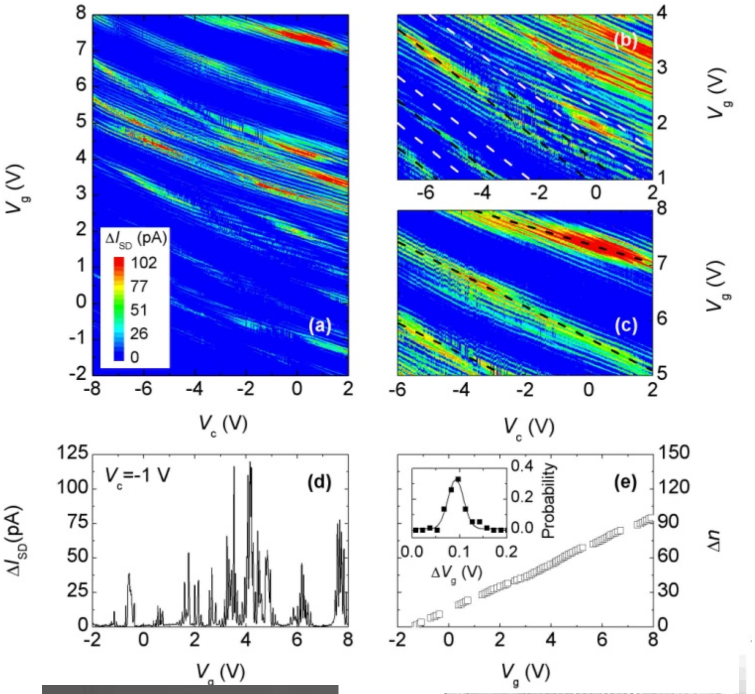
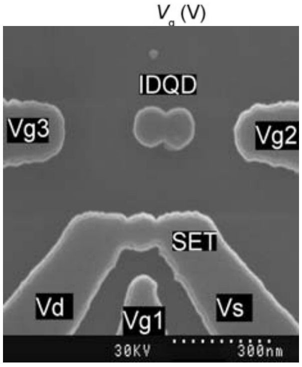
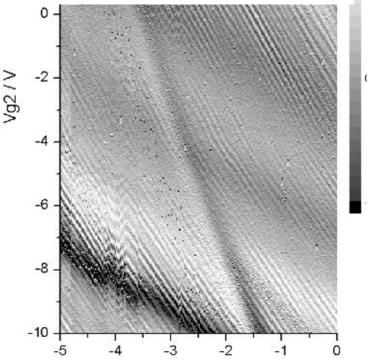
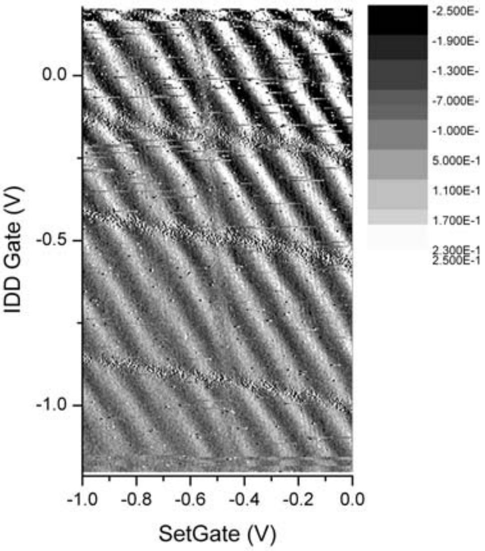
Left - typical results, showing structure attributable to the SET, to the IDQD, and to interactions between the two

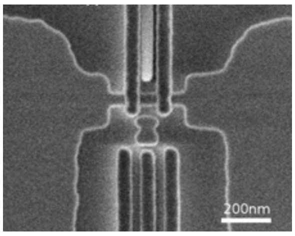


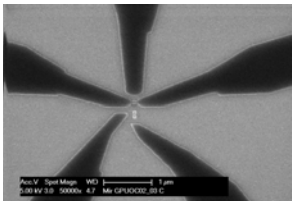
a) Gate dependency diagram
b) IDQD lines
c) Background conductance
d) Coulomb blockade oscillations
e) Periodicity and distribution











Devices with the same general structure of an isolated double-dot fabricated near a single-electron transistor electrometer are fabricated using a variety of technologies to evaluate the robustness of the designs.

Left - micrographs of device structures formed by three different processes. (Central micrograph courtesy of LETI, Grenoble.)

Above – results from two different devices showing superposed structure due to the SET and the IDQD.