Spin-functional MOSFETs

Satoshi Sugahara[1,2,3]

[1]Imaging Science and Engineering Laboratory, Tokyo Institute of Technology
[2]Department of Electronics and Applied Physics, Tokyo Institute of Technology
[3]CREST, Japan Science and Technology Agency

In the near future, the CMOS scaling will reach the physical limit of several nanometers. Therefore, scaling-independent technology to improve device performance attracts considerable attention. From this point of view, great efforts have been paid to achieve much higher current drivability of CMOS so far. Introduction of new functionality into CMOS is expected to be an alternate approach to improve circuit performance. Spin-functional MOSFETs are a new concept that unites an ordinary MOSFET with useful functions of recently emerging spintronic devices. Magnetic tunnel junctions (MTJs) are a key device for this concept owing to their unique functions of nonvolatile information storage and reconfigurable output characteristics. Figures 1 (a) and (b) show device and circuit approaches to realize spin-functional MOSFETs, respectively. Spin-MOSFET (S-MOSFET) with ferromagnetic source/drain (S/D) can merge the functions of MTJs into a MOSFET at device level. Pseudo-spin-MOSFET (PS-MOSFET) is a circuit approach to realize the functions of S-MOSFET using an ordinary MOSFET and MTJ, based on MRAM technology.

Figure 2 (a) shows the calculated output characteristics of an S-MOSFET with the half-metallic ferromagnet (HMF) S/D. HMFs have the spin polarization of 100% and are the most promising material for the spin injector/detector (S/D) of S-MOSFETs owing to the spin filter effect of HMFs with high efficiency. The S-MOSFET shows excellent transistor behavior in the parallel magnetization configuration (solid curves), and the drain current highly regulates in antiparallel magnetization (broken curves). Figure 2(b) shows the calculated output characteristics of an S-MOSFET using the ferromagnetic S/D with a spin polarization of 70%. The magnetization-configuration-dependent output characteristics are also established. Figure 3(a) shows the magnetocurent ratio γ_{MC} as a function of spin polarization of the ferromagnetic S/D, in which γ_{MC} is an index of performance of spin-transistor given by $\gamma_{MC} = (I_D^{P}-I_D^{AP}) / I_D^{AP}$. A moderate γ_{MC} value (~100%) is sufficient for logic applications discussed later. Therefore, extremely high spin polarization is not required. However, HMFs are still important as a high spin polarization (>70-80%) material (Note that these high spin polarization values are inaccessible to ordinary ferromagnets). Barrier height control for HMF/Si junctions is also important to realize a sufficient γ_{MC} value (Fig. 3(b)).

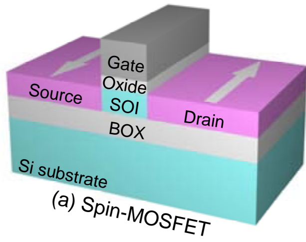
Ferromagnetic S/D technology using HMFs is the most important challenge to develop S-MOSFETs. Co-based full-Heusler alloys is a half-metallic ferromagnet with the higher Curie temperature than RT, and full-Heusler alloys containing Si are considered to be a kind of silicide that has possibility to be formed by CMOS silicidation process. We developed a new RTA-based preparation technique for full-Heusler alloy thin films employing SOI substrates. Full-Heusler alloys have the fully ordered $L2_1$ structure and also other disordered structures. It is well recognized that the disordered structures of full-Heusler alloys strongly affect their half-metallicity. Figure 4 shows the degree of atomic ordering of RTA-formed full-Heusler Co_2FeSi (CFS) films. The CFS films were the highly $L2_1$-ordered structure, and the degree of $L2_1$-odering was higher than 80% that was comparable to high quality bulk CFS. Barrier height control using dopant segregation technique is also applicable to our developed RTA technique for full-Heusler alloy thin films (Fig. 5)

Figure 6 shows the circuit configuration of PS-MOSFET. A MTJ connected to the source terminal of a MOSFET feeds back its voltage drop to the gate, and the degree of negative feedback depends on the resistance states of the MTJ. The actual input bias V_{GS0} and also body bias V_{BS0} can be varied by the magnetization configurations of the MTJ. Therefore, the PS-MOSFET can possess high and low current drivabilities that are controlled by the magnetization configurations of the MTJ, as shown in Fig 7. Furthermore, magnetic-field-free current-induced magnetization switching (CIMS) for the MTJ can be achieved by increasing V_G, as also shown in Fig. 7. Thus, the PS-MOSFET can reproduce the spin-transistor behavior and would be the most promising spin-transistor based on present MRAM technology. Figure 8 shows γ_{MC} as a function of tunneling magnetoresistance ratio TMR, in which resistance R_P of the MTJ in parallel magnetization is varied. Desired γ_{MC} can be easily designed by adjusting TMR and R_P. However, it should be noted that high R_P degrades the current drivability of the PS-MOSFET.

In order to demonstrate spin-transistor actions of PS-MOSFET, a prototypic PS-MOSFET was fabricated using a spin-valve-type MTJ with a full-Heusler alloy (Co_2FeAl; CFA) electrode and MgO tunnel barrier. Figure 9 shows the drain current as a function of magnetic field. The drain current well reflects the resistance change of the MTJ. γ_{MC} was 15% at drain bias V_D of 0.5V and gate bias V_G of 5V. γ_{MC} increased with decreasing V_D and increased with increasing V_G. The maximun γ_{MC} value was as high as 50%.

Nonvolatile logic devices such as nonvolatile SRAM (NV-SRAM) and nonvolatile flip-flop (NV-FF) are one of the most important applications for PS-MOSFETs. NV-SRAM can be simply configured by connecting two PS-MOSFETs to the storage nodes of a standard SRAM cell, as shown in Fig. 10(a). Figure 11 shows the simulated wave form for store and restore operations of the NV-SRAM cell. The cell can be shut down without losing its logic information. NV-FF can be also configured in the same manner (Fig. 10(b)). These NV-SRAM and NV-FF are required as key devices for ideal power-gating system that is expected to be promising architecture to drastically reduce static power dissipation in CMOS logic/processor (Fig. 12).

References: [1] S.Sugahara, IEE Proc. Circuits, Device-Systems **152**, 355 (2005). [2] S.Sugahara, Physica Status Solidi C **3**, 4405 (2006). [3] Y. Takamura *et al*, J. Appl. Phys. **103**, 07D719 (2008). [4] Y. Takamura *et al*, J. Appl. Phys. **105**, 07B109 (2009). [5] S.Yamamoto *et al*, Jpn. J. Appl. Phys. **48**, 043001(2009). [6] Y.Shuto *et al*, J. Appl. Phys. **105**, 07C933 (2009). [7] Y. Takamura *et al*, Intl. Symp. Silicon Nanodevices in 2030, Tokyo, 2009. [8] Y. Shuto *et al*, Intl. Symp. Silicon Nanodevices in 2030, Tokyo, 2009.



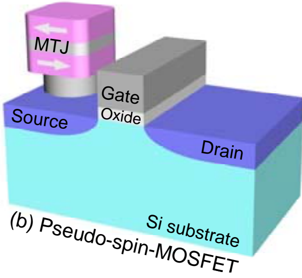
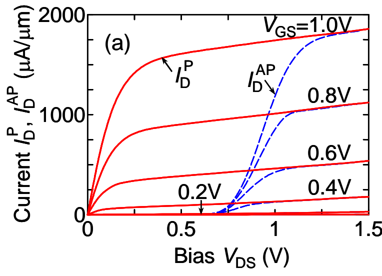


Fig. 1



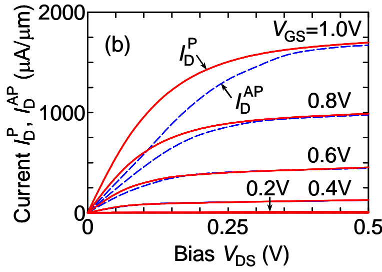
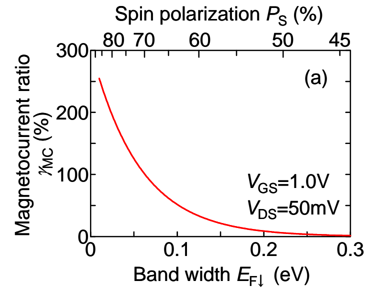


Fig.2



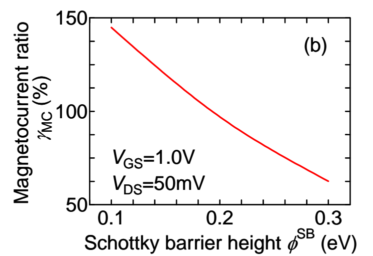


Fig.3

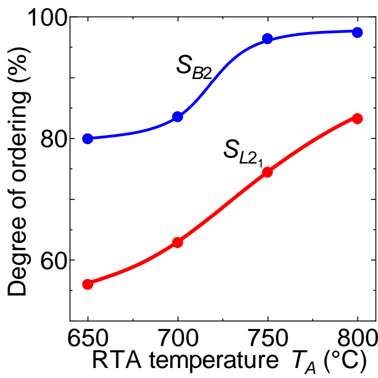


Fig.4

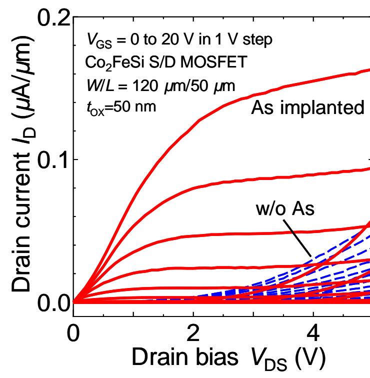


Fig.5

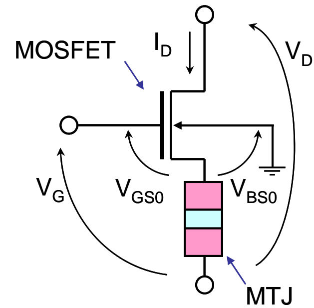


Fig.6

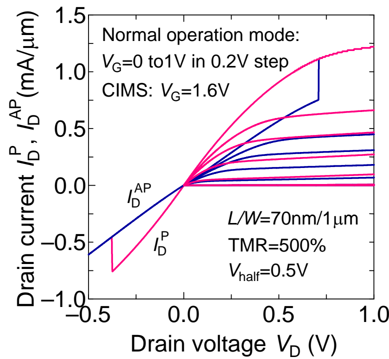


Fig.7

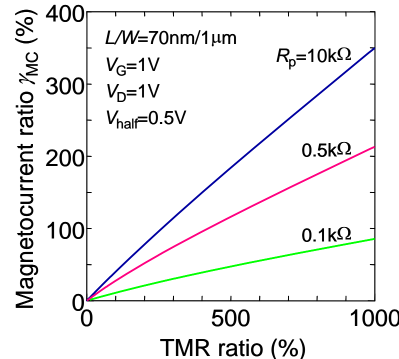


Fig.8

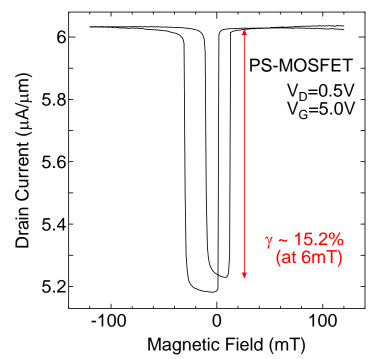


Fig.9

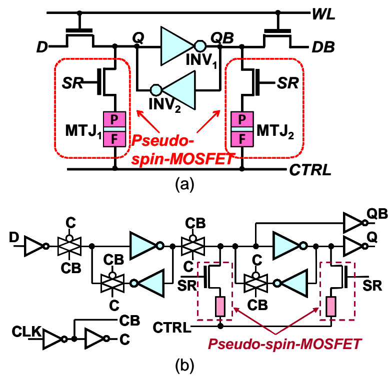


Fig.10

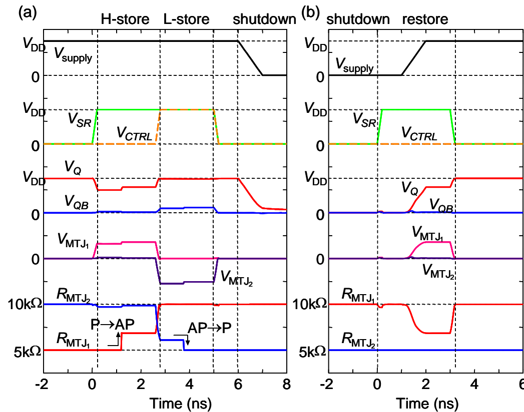


Fig.11

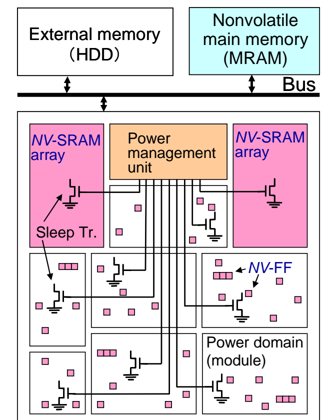


Fig.12