Trends and prospects of Si devices for LSI applications

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Since the transistor dimensions have been scaled beyond 90nm technology node, the traditional scaling strategy, namely scaling of transistor dimensions, is not enough to achieve required transistor performance. Therefore, a number of new performance booster technologies such as stain, high-κ gate dielectric, and metal gate electrode, have been introduced in advanced devices. The SOI technology is also utilized because the SOI structure is advantageous in terms of parasitic capacitance as well as electrostatics. Particularly, three-dimensional structures such as FinFETs and nano-wire transistors are promising because of their excellent electrostatics. However, there are some obstacles to be overcome. The three-dimensional structures have worse parasitic capacitance/resistance. The quantum mechanical effects in these structures should be well understood in order to utilize them in VLSI products. Furthermore, because multiple surface orientations are utilized in three-dimensional FETs, carrier transport in surface orientations other than (100) should be fully understood.

In this work, quantum mechanical effects and carrier transport in nanoscaled SOI structures will be extensively discussed. Uniaxial stress engineering is another key technology to improve CMOS performance. The physical mechanisms of electron mobility (μ_e) enhancement by uniaxial stress are experimentally and theoretically investigated in bulk (100) and (110) nMOSFETs. It is experimentally demonstrated that the energy surface of the 2-fold valleys in (001) FETs is warped due to uniaxial <110> stress, resulting in lighter transverse effective mass (m_T) along the stress direction. It is also shown that the lighter m_T benefits <110> uniaxial stress in terms of μ_e enhancement particularly at higher stress. New channel materials for VLSI applications will be also discussed. Finally, Si devices in future VLSIs will be prospected.