Physics for Si nanowire FET and its fabrication

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Recent LSI technologies require the introduction of a wide variety of materials and structures in addition to conventional aggressive down-scaling. As a result, present semiconductor devices contain various kinds of nano-structures. As for future Si nano-electronics, Si nanowire FET is expected to be one of the most promising structures, since nanowire structure can suppress the off-current. However, guiding principles for designing Si nanowire FET are not well established. In this presentation, we try to propose guiding principles toward future Si nanowire FET based on atomic and electronic structures of Si nanowire.

Although nanowire structure can suppress off-current, the total current required for driving the circuit would be limited due to its narrower cross section. One way to increase the on-current at small cross section is to achieve ideal one-dimensional transport limit (Landauer limit). To achieve Landuer limit, however, narrower Si NWs which has a small number of quantum channels are necessary. First, we point out the existence of the optimal nano-wire size based on the first principles band structure calculations.

Band structures of SiNWs with 0.77 and 2.30 nm are shown in Fig. 1 [1]. SiNWs with theses dimensions have direct band gap at Γ point, which are in contrast to the indirect band structure of bulk Si, reproducing the reported first principles calculations [2]. When one-dimentional ballistic conduction is achieved, the conductivity of SiNW MOSFET is basically determined by the number of quantum channels near conduction band minimum (CBM) and valence band maximum (VBM). Here, the numbers of quantum channels within 50 meV from the valence band top (number of hole channels) are plotted in Fig. 2. Number of hole channels increases from 2 to 7, as the SiNW size increases from 0.77 nm to 3.84 nm. Therefore, larger SiNW size can achieve higher conductivity from the viewpoint of the number of quantum channels. However, as the density of bands increase, the spacing of each band becomes narrower, which will allow inter sub-band scattering and eventually reduces the conductivity [3]. In the light of the above discussions, it may be concluded that there exists a trade off between the quantum channel numbers and inter sub-band scattering and an optimum size exists for MOSFET application (Fig. 3) [1].

Moreover, we also propose the optimal Si oxidation procedures for Si nanowire FET based on the Si emission model (Fig. 4) [4].

References

[1] Y. Lee, et al. ECS Trans. **16**, 1 (2009).
[2] T. Ohno, K. Shiraishi and T. Ogawa, Phys. Rev. Lett. **69,** 2400 (1992).
[3] H. Sakaki, Jpn. J. Appl. Phys. **19,** L735, (1980).
[4] H. Kageshima and K. Shiraishi, Phys. Rev. Lett. **81,** 5936, (1998).

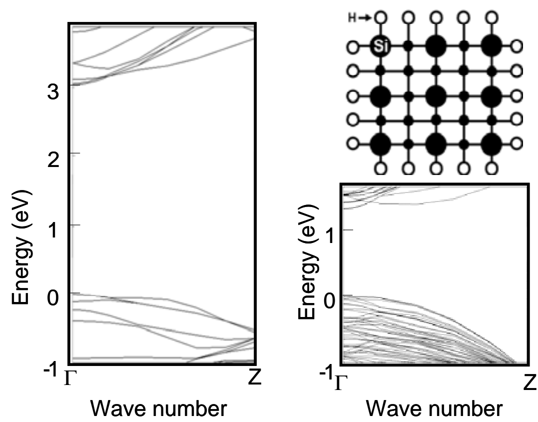

Fig. 1: Band structures of Si NW with the width of 0.77 nm (left) and 2.3 nm (right).

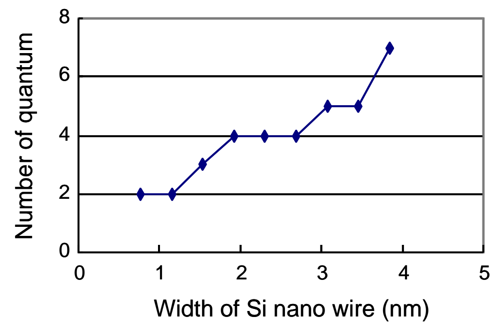

Fig. 2: The number of quantum channels plotted as a function of Si nano-wire width.. The numbers of quantum channels within 50 meV from the valence band top (number of hole channel) is given.

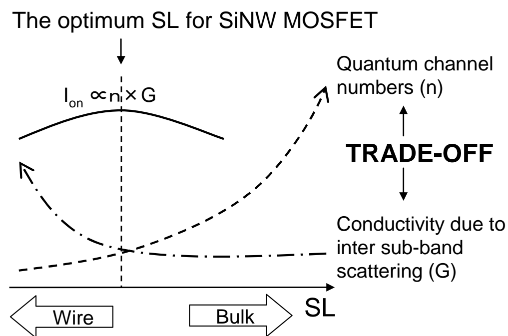

Fig.3: The trade off model between the quantum channel numbers (n) and the conductivity (G) with inter sub-band scattering. The arrow of n and G curves points a direction to obtain a high I_{on}. An optimum Si nano-wire size should exist.

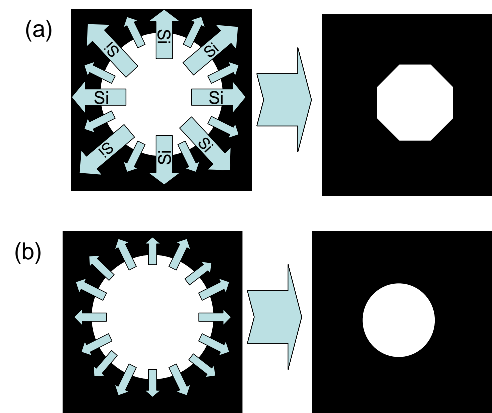

Fig. 4: Facet formation mechanism (a) and recipe for uniform oxidation. (b) (a) The surface with large Si emission rate tends to be a facet as the oxidation proceeds. (b) Suppression of Si emission (suppression of oxidation induced strain) leads to uniform oxidation.